REMARKS

The Office Action dated September 28, 2005, has been received and carefully noted. The above amendments to the claims, and the following remarks, are submitted as a full and complete response to the Office Action.

Claims 1, 8, 13, 28, 32, 52 and 57 are amended to particularly point out and distinctly claim the subject matter of the present invention. No new matter is added. Support for the amendments is found at least on page 8 lines 1-12 of the specification and Figure 4. Entry of the amendments is respectfully requested because the amendments do not require further search or consideration, and place the application in condition better condition for appeal. Claims 1-60 are presently pending in the subject application and are respectfully submitted for consideration.

Claims 1-60 were rejected under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 6,021,132 to Muller et al. (Muller) in view of U.S. Patent No. 6,529,519 to Steiner et al. (Steiner), and further in view of U.S. Patent No. 5,860,136 to Fenner (Fenner). The Office Action took the position that Muller taught all the elements of the claims 1-60, with the exception of a single buffer per packet mechanism and an index key. Steiner was cited as providing the single buffer per packet mechanism and Fenner was cited as providing the index key. Applicants respectfully submit that Muller, Steiner and Fenner, either alone or in combination, fail to disclose or suggest all the features of any of the presently pending claims.

Claim 1, upon which claims 2-7 are dependent, recites a memory structure. The memory structure includes an Address Resolution Table for resolving addresses in a packet-based network switch and using a key to index a location within the Address Resolution Table wherein the key is a predefined portion of a packet destination address. The memory structure also includes a Packet Storage Table, the Packet Storage Table adapted to receive a packet for storage in the packet-based network switch, and sharing a preselected portion of memory with the Address Resolution Table. The memory structure also includes a single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit descriptor read per the individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key. The entire packet is to be transmitted.

Claim 8, upon which claims 9-12 are dependent, recites a memory structure. The memory structure includes an Address Resolution Table having an associative memory structure and using a key to index a location within the Address Resolution Table. The Address Resolution Table resolves addresses in a packet-based network switch. The memory structure also includes a single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit descriptor read per the individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key, wherein the key is a predefined portion of a packet destination address.

Claim 13, upon which claims 14-27 are dependent, recites a memory structure having a memory block. The memory structure includes an Address Resolution Table having an associative memory structure. The Address Resolution Table resolves addresses in a packet-based network switch and using a key to index a location within the Address Resolution Table. The memory structure also includes a Transmit Descriptor Table. The Transmit Descriptor Table is associated with a corresponding packet-based network transmit port, and the Transmit Descriptor Table is adapted to receive a Table Descriptor Address and a Table Descriptor Value. The memory structure also includes a Packet Storage Table. The Packet Storage Table is adapted to receive at least one of each of a Packet Data Address portion and a Packet Data Value portion. The memory structure also includes a single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit descriptor read per the individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key wherein the key is a predefined portion of a packet destination address.

Claim 28, upon which claims 29-31 are dependent, recites a packet-based switch. The packet-based switch includes a shared memory structure having an Address Resolution Table and a Packet Storage Table. The packet-based switch also includes a key to index a location within the Address Resolution Table wherein the key is a predefined portion of a packet destination address. The packet-based switch also includes a single buffer per packet mechanism configured to receive an individual packet

for enabling only one transmit descriptor read per the individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key. The entire packet is to be transmitted.

Claim 32, upon which claims 33-51 are dependent, includes some of the features of claim 13, but is drawn to a packet-based switch.

Claim 52, upon which claims 53-56 are dependent, includes some of the features of claim 8, but is drawn to a packet-based switch.

Claim 57, upon which claims 58-60 are dependent, includes some of the features of claim 8, but is drawn to a packet-based switch.

As discussed in the specification, examples of the present invention enable a memory structure to resolve addresses in a packet-based network switch. Examples of the present invention enable bandwidth savings that are attributed to a one buffer-per-packet approach. The single buffer-per-packet approach enhances the feasibility of a bit-per-buffer pool tracking technique and the need to search a larger buffer structure can be mitigated or eliminated. Thus, a packet-based switch performs one memory read for address resolution, and one memory write for address learning, to the address table for each frame received. Overhead is reduced and a reduction in accesses per frame is achieved. The single access for both read and write can be attributed to the single-entry direct-mapped address table. Applicant respectfully submits that the cited references of Muller, Steiner and Fenner, when viewed alone or combined, fail to disclose or suggest

all the elements of the presently pending claims. Therefore, the cited references fail to provide the critical and unobvious advantages discussed above.

Muller relates to shared memory management in a switch network element. Muller describes a shared memory manager 220 that is exploited by input and output ports 206 by locally storing pointers to buffers that contain packet data rather than locally storing the packet data. A predetermined number of buffer pointers are kept on hand to allow immediate storage of received packet data. The buffer pointers are preallocated during the initialization of switching element 100 and requested from shared memory manager 220. Pointers are queued to buffers that contain packet data, and not to the packet data itself. Further, a packet can be stored over more than one buffer. Each buffer in shared memory 230 is owned by one or more different ports at different points in time without having to duplicate the packet data.

Steiner relates to prioritized-buffer management for fixed size packets in a multimedia application. Steiner describes a memory system that includes a tag register for storing tags associated with respective pages, wherein each tag indicates whether the associated page is empty or full. Steiner also describes a shadow register for storing conflict-free updates from the tag register and a page register for storing pointers to the lowest free or unoccupied page. Steiner also describes a buffer that is organized along packet boundaries or pages for convenience of operation. A processor maintains a table of pointers to each packet boundary, and, therefore, knows the location of all leftover

packets. A tag register 40 is provided, that has as many bits as there are packet boundaries of buffer 22.

Fenner relates to a method and apparatus for use of associated memory with large key spaces. Fenner describes an associative memory that utilizes a location addressable memory and a lookup table to generate, from a key, the address in memory storing an associated record. Fenner describes an associative memory utilizing arithmetic coding to associate a key presented to the memory with a record stored in the memory. The associative memory includes an index table stored in memory and a record memory for storing the records of data. The index table is constructed so that each symbol of a key, with a key being divided into a string of symbols and each symbol being defined by its position within the key and its value, addresses an index value in the index table memory. The index values are assigned such that the sum of index values for a given key is a unique value that is used to address the record memory.

Applicants submit that the cited references taken individually or in combination fail to disclose or suggest at least the feature of a Packet Storage Table adapted to receive a packet for storage in the packet-based network switch and sharing a pre-selected portion of memory with the Address Resolution Table, as recited in claim 1 (underline added).

Instead, Muller discloses shared memory 230 in which services two types of clients, buffer consumers (input ports) and buffer providers (output ports). See column 8 lines 22-30. Muller, fails to even mention the feature that a pre-selected portion of

memory is shared by the Address Resolution Table and the Packet Storage Table as clearly recited in claim 1.. Similarly, neither Steiner nor Fenner mentions, discloses or suggests this feature and therefore, fail to make up for the deficiencies of Muller.

Further, Applicants submit that the cited combination of references fail to disclose or suggest at least the feature a single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit descriptor read per said individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key, wherein the entire packet is to be transmitted, as recited in claim 1 and similarly recited in claims 8, 13, 28, 32, and 57.

The Office Action admits that Muller fails to disclose this feature and alleges that Steiner and Fenner make up for this deficiency. However, Applicants submit that Steiner and Fenner fail to make up for the admitted deficiencies of Muller. Specifically, Steiner does not mention, disclose or suggest execution of a single access in order to locate an entire packet at the location using the key, wherein the entire packet is to be transmitted (underline added). The portions of Steiner cited in the Office Action (col. 7 line 63- col. 8 line 3 i.e., claim 1) at best, merely recite a means for generating a succession of addresses of memory locations which control sequential writing into the buffer of bytes contained in data packets and jumping over addresses within pages which are full, thereby bypassing and avoiding overwriting pages which are full.

Fenner merely discloses a key, which is used via arithmetic coding to create an index table, wherein the sum of index values for a given key is used to address a record

memory. See Fenner column 6 lines 34 -50 and column 18 lines 43-51. Thus, neither of these references taken individually or in combination, discloses or suggests execution of a single access in order to locate an entire packet at the location using the key, wherein the entire packet is to be transmitted, as recited in the pending claims.

Still further, the key disclosed in Fenner is a compressed version of the entire destination address and is not therefore, a pre-selected portion of the destination address, as recited in the current claims. The pre-selected portion is the least significant bits of the destination address. As stated above, see page 4 lines 1-12 of the specification.

Based at least on the above, Applicants submit that the cited references taken individually or in combination, fail to disclose or suggest all of the features recited in any of the pending claims. Accordingly, withdrawal of the rejection of claims 1-60 under 35 U.S.C. §103(a) is respectfully requested.

As discussed above, in the present invention the single access for both read and write can be attributed to the single-entry direct-mapped address table.

For at least these reasons, applicants submit that the cited references, either alone or in combination, do not disclose or suggest at least these features of claims 1-60. Applicants respectfully request that the obviousness rejection be withdrawn.

It is further submitted that each of claims 1-60 recites subject matter that is neither disclosed nor suggested by the cited references. It is therefore respectfully requested that all of claims 1-60 be allowed, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,

David E. Brown
Registration No. 51,091

Customer No. 32294
SQUIRE, SANDERS & DEMPSEY LLP
14TH Floor
8000 Towers Crescent Drive
Tysons Corner, Virginia 22182-2700
Telephone: 703-720-7800
Fax: 703-720-7802

DEB/cvl